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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,497	07/17/2003	Tetsuhiro Iwai	35908	2610
116	7590	12/07/2005	EXAMINER	
PEARNE & GORDON LLP 1801 EAST 9TH STREET SUITE 1200 CLEVELAND, OH 44114-3108			VINH, LAN	
			ART UNIT	PAPER NUMBER
			1765	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/621,497	IWAI ET AL.
	Examiner Lan Vinh	Art Unit 1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 31 August 2005.

2a) This action is **FINAL**.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 6-8 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 6-8 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Kakehi et al (US 4,565,601)

Kakehi discloses method for controlling sample temperature in plasma etching. The method comprises the steps of:

placing a substrate 50 on a conductive electrode 20 (col 3, lines 61-63), the electrode 20 has a top surface that is greater in external size than a substrate to be plasma-processed (fig. 1), the substrate has an insulating layer on a front surface thereof (col 9, lines 28-30), the top surface of the electrode has a top surface central area that is inside a boundary line that is distant inward by a prescribed length from an outer periphery of the substrate and in which the electrode/conductor is exposed (fig. 1; fig. 7), a ring-shaped top surface peripheral area 120 that surrounds the top surface central area (fig. 8), the electrode/conductor is covered with an insulating coating 60 (col 5, lines 36-39) , plasma processing is performed in a state that the substrate is held by the top surface of the electrode by electrostatic absorption (col 5, lines 18-22), the electrode is being cooled (col 5, lines 55-58), the substrate 50 is mounted on the top surface of the electrode in such a manner that a central portion and a peripheral portion of the

insulating layer of the substrate are in contact with the top surface central area and the insulating coating in the top surface peripheral area ( fig. 1), the substrate is electrostatically absorbed on the top surface central area by mainly utilizing the central portion of the insulating layer as a dielectric for electrostatic absorption (col 7, lines 28-31), the top surface central area of the electrode 20 is insulated from plasma by bringing the outer peripheral portion of the insulating layer into close contact with the insulating coating (fig. 4)

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 7-8 rejected under 35 U.S.C. 103(a) as being unpatentable over Kakehi et al (US 4,565,601) in view of Desalvo et al (US 6,884,717)

Kakehi method has been described above. Unlike the instant claimed inventions as per claims 7-8, Kakehi fails to disclose that the semiconductor substrate has logic circuit formed on the front surface and etching away the back surface of the substrate

Desalvo discloses a method for etching semiconductor wafer that has logic circuit formed on the front surface and thinning /etching away the back surface of the semiconductor wafer (col 4, lines 51-54; fig. 1)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Kakehi method by adding the step of thinning /etching away the back surface of the semiconductor wafer as per Desalvo because Desalvo discloses that the use of etching for wafer thinning enables the formation of desirable physically strengthening shapes in the backside material and preventing wafer breakage (col 4, lines 55-60)

### ***Response to Arguments***

5. Applicant's arguments filed 8/31/2005 have been fully considered but they are not persuasive.

Applicants argue that Kakehi does not disclose or suggest all the elements of the claimed invention since the entire Kakehi upper plate electrode is coated with an insulating film Kakehi does not teach a top surface central area in which the conductor is exposed and a ring-shaped top surface peripheral in which the conductor is covered with an insulating covering. This argument is unpersuasive because while it is true that Kakehi discloses that the entire upper plate electrode is coated with an insulating film, it is also true that in one of the embodiment, Kakehi discloses that a top surface central area in which the electrode/conductor is exposed (the top surface central area of electrode 26' is exposed through a gap between the electrode and the cover 110 as seen in fig. 7) and a ring-shaped top surface peripheral in which the electrode/conductor is covered with an insulating covering (col 8, lines 20-25). Thus, it is asserted that Kakehi discloses a top surface central area in which the conductor is exposed and a

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ring-shaped top surface peripheral in which the conductor is covered with an insulating covering as required in claim 6

The applicants also argue that since the entire substrate surface is mated to the insulating film of the Kakehi upper plate electrode, Kakehi does not teach that a central portion of the substrate is in contact with the top surface central area of the electrode and a peripheral portion of the substrate is in contact with the top surface peripheral area of the electrode. This argument is unpersuasive because while it is true that the entire substrate surface is mated to the insulating film of the Kakehi upper plate electrode, it is also true that in Kakehi, a central portion of the substrate 50 is shown in contact with the top surface central area of the electrode 26' (fig. 7), and a peripheral portion of the substrate 50 is shown in contact with the top surface peripheral area of the electrode 20. Thus, it is asserted that Kakehi discloses that a central portion of the substrate is in contact with the top surface central area of the electrode and a peripheral portion of the substrate is in contact with the top surface peripheral area of the electrode

**6. THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471.

The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LV  
December 1, 2005